

FIG. 2

oedere zerrede

cecs and and aco

**ADDRESS** 

FFFFFFF	DECED//ED			
FFFFE000	RESERVED			
FFFFDFFF				
FFFFD400	DSP MODULE			
FFFFD3FF	INTERNAL DAM ARRA			
FFFFD000	INTERNAL RAM ARRAY			
FFFFCFFF	RESERVED			
01000000	NESERVED			
00FFFFFF	INTERRUPT CONTROL			
00FFFE00	INTERRUPT CONTRO			
00FFFDFF	EXTERNAL			
00000000	MEMORY AND I/O			
•				

FIG. 5

## D Re(D[0]) D+2 Im(D[0]) D+4 Re(D[1]) D+6 Im(D[1]) : D+4n Pe(D[n]) FIG. 6

**CONTENTS** 

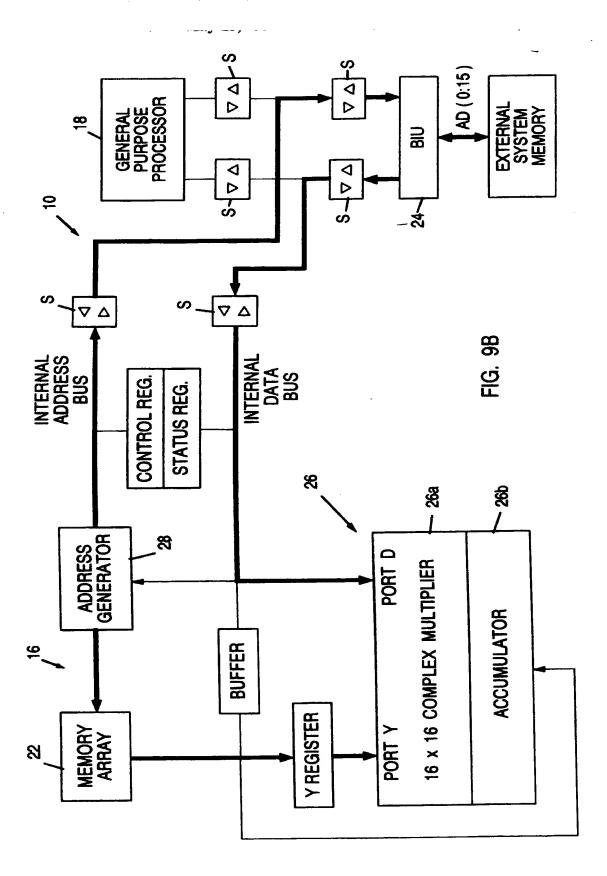
INSTRUCTION	OPC1	OPCO CLR COJ	C.B.	g	OPERATION	CYCLES
	0	0	0	0	C[i] <= C[i] + Y x D[i]	
c	0	0	0	-	C[i] <= C[i] + Y x D[i] *	(8 × N / 10
	0	0	-	0	C[i] <= YxD[i]	(0 < 2 ) + 0
	0	0	<del>-</del> .	<del></del> -	C[i] <= Y x D[i] *	
	0	-	0	0	C[i] <= C[i]x(1+D[i])	
;	0	-	0	-	C[i] <= C[i]x(1+D[i]*)	(8×N) +6
VCMUL	0	<del></del>	-	0	C[i] <= C[i] x D[i]	
	0	<del></del>	•	-	C[i] <= C[i] xD[i] *	
	-	0	0	0	A <= A + SIGMA(C[i]xD[i])	
	_	0	0	0	A <= A + SIGMA(C[i]xD[i]*)	
VCMAC	<b>-</b>	0	-	0	A <= SIGMA(C[i]xD[i])	(8×N) +9
	-	0	<del></del>	<del></del>	A <= SIGMA (C[i] x D[i] *)	
	-	-	0	0	A <= A + SIGMA (C[i]xC[i] )	
		-	0	<del></del>	A <= A + SIGMA (C[i]xC[i]*)	
VCMAG	_	-	<del></del>	0	A <= SIGMA(C[i]xC[i])	(8×8) +c
	_	-	•	-	A <= SIGMA(C[i]xC[i]*)	

F. 7

INCREMENTED ADDRESS BITS	A1 – A4	A1 – A5	A1 – A6	A1 – A7
CONSTANT ADDRESS BITS	A0 , A5 – A23	A0, A6 - A23	A0, A7 – A23	A0 , A8 – A23
EXTERNAL BUFFER SIZE ( DM )	∞	16	32	2
DSO	0	-	0	<del>-</del>
DS1	0	0	-	-

FIG.8

COBULLEY DIEDOS



ooruuter carooo

DOBULLEY DIEDOS